REMARKS

Claims 1-4, 6-13, 15-21, 24 and 25 were examined and rejected. Applicants cancel claims 1-4, 6-7 and 20-21. Applicants amend claims 8 and 11. Applicants submit that no new matter is added therein, as the amendments to claims 8 and 11 are at least supported by Figures 3-5 and paragraphs 18, 25, 33-34, and 42-43 of the application, as originally filed. Applicants respectfully request reconsideration of amended 8-13 and 15-19 in view of the following remarks.

I. Claims Rejected Under 35 U.S.C. § 102

The Patent Office rejects claims 1-2 and 6-7 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,119,192 to Kao et al. (Kao). It is axiomatic that to be anticipated every limitation of the claim must be disclosed in a single reference.

Applicants cancel claims 1-2 and 6-7.

II. Claims Rejected Under 35 U.S.C. § 103

The Patent Office rejects claims 3-4 under 35 U.S.C. § 103(a) as being unpatentable over Kao in view of U.S. Patent Application No. 2004/0143715 to Bonaccio et al. (Bonaccio). To render a claim obvious, every limitation of that claim must be taught or suggested by at least one properly combined reference.

Applicants cancel claims 3-4.

The Patent Office rejects claims 8-10 under 35 U.S.C. § 103(a) as being unpatentable over Kao in view of Bonaccio, and U.S. Patent No. 6,480,946 of Tomashima et al. (Tomashima).

Applicants disagree with the rejection above for claim 8 for at least the reason that the references do not teach or enable repeating the resetting and loading of a test device from a non-volatile test memory at least three times to repeat a multi-stage test data loading process with subsequent test information stored in the non-volatile

memory during a memory design validation stage, then manufacturing a plurality of products based on the subsequent test information, as required by amended claim 8.

Kao discloses an interface and memory for providing second initialization parameters from a supplemental parameter memory separate and distinct from the system BIOS memory (see column 2 lines 63-67). Specifically, Kao only teaches and only enables loading second initialization parameters from an I2C bus, and loading first initialization parameters from BIOS (see column 2 line 55 through column 3 line 60).

In addition, Bonaccio fails to cure the shortcomings of Kao. Bonaccio teaches reconfiguring an integrated circuit by retrieving and loading register settings (see Abstract).

In addition, Tomashima fails to cure the shortcomings of the other references. Tomashima teaches reducing skew between read and write communications signals of a memory system including a plurality of discrete memory devices connected in parallel to a bus to transmit/receive signals to and from a commonly provided controller (see column 1 lines 7-15; column 6 lines 44-53). Also, Tomashima teaches a conventional memory controller performing this reduction in communications signal skew by sending a command signal to Vernier circuit 300a during initialization of the memory devices (see column 6 lines 60-65; column 7 lines 30-33) during normal operational mode (see column 37 lines 33-39; column 8 lines 57-62; column 36 line 26 through column 37 line30; and column 38 lines 1-4).

However, the Patent Office has not identified and Applicants are unable to find any teaching or enablement in the references of repeating the resetting and loading of a test device from a non-volatile test memory at least three times to repeat a multi-stage test data loading process with subsequent test information stored in the non-volatile memory during a memory design validation stage, then manufacturing a plurality of products based on the subsequent test information, as required by amended claim 8.

Moreover, there is no enablement in Tomashima (or the combination of references) of the claimed requirement of resetting configuration registers and loading configuration registers using information stored in a nonvolatile memory.

In addition, by repeating the resetting and loading of a test device from a non-volatile test memory at least three times to repeat a multi-stage test data loading process with subsequent test information stored in the non-volatile memory during a memory design validation stage, then manufacturing a plurality of products based on the subsequent test information, embodiment described in the specification, for example, without limitation thereto, provide benefits of allowing a designer to test configurations of devices in the laboratory so that end user products can be designed and manufactured to requiring less memory (e.g., BIOS) and cost (see at least ¶¶ [0003], [0017]-[0021], [0025], and [0042]-[0043] of the Application). However, none of the references teach or enable such benefits.

Moreover, Applicants submit that the combination of Tomashima with Bonaccio or Kao is improper. Specifically, Bonaccio and Kao teach configuration data sets stored in BIOS and used to program configuration registers. On the other hand Tomashima teaches reducing a communications channel skew by adjusting reference voltage Vref of a Vernier circuit to reduce skew between read and write signals to and from discrete memory devices of a memory system (see Figures 43 and 46; and column 35 line 28 through column 37 line 55). Vref is updated using tap circuit 300a which includes a shift register circuit 315, gates, latches and switches (see column 38) which may be initialized by a command applied from the memory controller (see column 37 lines 1-10). Thus, the combination is improper for the first reason that Tomashima is in the field of volatile RAM system memory, but is not in the non-volatile BIOS memory field of Kao and Bonaccio. Second, the combination is improper for the second reason that Tomashima is in the field of correcting communication channel skew errors, but it is not in the BIOS program data field of Kao and Bonaccio. Third, as noted there is no motivation or enablement in Tomashima for resetting configuration registers and loading configuration registers using information stored in a nonvolatile memory. Thus, the motivation for such a combination can be gleaned only from Applicants' specification. Hence, the combination is improper. Therefore, for at least these additional three reasons, Applicants respectfully request the Patent Office withdraw the rejections herein based on these references.

Hence, for at least these reasons, Applicants respectfully request the Patent Office withdraw the rejection above for claim 8.

The Patent Office rejects claims 11-13, 15-19, 24 and 25 under 35 U.S.C. § 103(a) as being unpatentable over Kao in view of Bonaccio, U.S. Patent No. 6,480,946 of Tomashima et al. (Tomashima), and Official Notice.

Applicants respectfully disagree with the rejection above for claim 11 for at least the reason that the cited references do not teach or enable: b) storing test information associated with the desired configuration in a memory; c) resetting each of the plurality of registers to a register default data value; d) loading the registers according to the test information during a memory design validation stage; e) identifying a subset of the plurality of test data that equal to desired data for achieving the desired configuration prior to loading; f) repeating b), c), d) and e); then g) manufacturing a plurality of products based on the test information and the subset, as required by amended claim 11.

Arguments analogous to the ones above for claim 8 apply to show that Kao, Bonaccio and Tomashima do not teach or enable the corresponding above noted limitations required by claim 11, or benefits thereof.

Moreover, Arguments analogous to the ones above for claim 8 apply to show that the combination of Tomashima with Bonaccio or Kao is improper.

In addition to the reasons above, Applicants traverse the Official Notice that the combined teachings of Tomashima, Bonaccio and Kao can be combined with well known teachings of manufacturing based on test validation data, and respectfully request that the Patent Office cite a reference in support of that position, in accordance with MPEP § 2144.03.

Moreover, as noted above and in the Examiner's current intended use rejections of claims 1-2 and 6-7, Tomashima, Bonaccio and Kao only teach end user products, but do not teach testing prior to manufacture. Thus, the combination of Tomashima, Bonaccio or Kao with any teaching of manufacturing based on test validation data is improper.

Hence, for at least these reason, Applicants respectfully request the Patent Office withdraw the rejection above of claim 11.

The Patent Office rejects claims 20 and 21 under 35 U.S.C. § 103(a) as being unpatentable over Kao in view of Bonaccio and U.S. Patent No. 5,737,524 to Cohen et al. (Cohen).

Applicants cancel claims 20-21.

Any dependent claims not mentioned herein are submitted as not being anticipated or obvious for at least the reasons given above in support of their base claims and for the additional further limitations of those dependent claims.

Hence, Applicants respectfully request the Patent Office withdraw the rejection above of all the claims.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 8/14/2008

Angelo J. Gaz, Reg. No. 45,907

1279 Oakmead Parkway
Sunnyvale, California 94085-4040
Telephone (310) 207-3800
Facsimile (408) 720-8383

CERTIFICATE OF TRANSMISSION
I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below to the United States Patent and Trademark Office.

Nedy Calderon 8/14/08

Nedy Calderon Date